PRODUCT RELIABILITY REPORT

Platform: S100E3.0I

--100V E-Mode GaN FET

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1. Platform Information

Platform	S100E3.0I
BV Rating(V)	100
Process Technology	GaN on Silicon

2. Reliability Tests

Innoscience's E-mode GaN FET was subjected to a variety of reliability tests under the conditions referenced to typical for silicon-based power MOSFET.

Category	Product Name	Package	BV Rating(V)
Platform	INN100EA035A	En-FCLGA 3.3X3.3	100

Platform reliability test items and results were shown as below:

Platform Product (INN100EA035A) qualification result				
Test Items	**Test Condition**	**#Fail**	**Sample Size (Unit x Lot)**	**Result**
HTRB	T=150°C, VD=100V, 1000hrs	0 Fail	77 x 3	Pass
LTRB	T=-40°C, VD=100V, 1000hrs	0 Fail	77 x 3	Pass
HTGB	T=150°C, VG=6V, 1000hrs	0 Fail	77 x 3	Pass
HTGB-	T=150°C, VG=-4V, 1000hrs	0 Fail	77 x 3	Pass
LTGB	T=-40°C, VG=6V, 1000hrs	0 Fail	77 x 3	Pass
LTGB-	T=-40°C, VG=-4V, 1000hrs	0 Fail	77 x 3	Pass
ESD-HBM	T=25°C, All pin	0 Fail	10 x 1	Class_1B
ESD-CDM	T=25°C, All pin	0 Fail	10 x 1	Class_C2a
DHTOL	Hard switching, T=125°C, 100KHz, VD=80V, 1000hrs	0 Fail	8set x 1	Pass
	Hard switching, T=125°C, 600KHz, VD=80V, 1000hrs	0 Fail	8set x 2	Pass
	Soft Switching, T=125°C, 500KHz, VD=80V, 1000hrs	0 Fail	8set x 1	Pass
	Soft Switching, T=125°C, 1.5MHz, VD=80V, 1000hrs	0 Fail	8set x 2	Pass
MSL3	T=30°C, RH=60%, 3 x reflow, 192hrs	0 Fail	25 x 3	Pass
H^3TRB	T=85°C, RH=85%, VD=80V, 1000hrs	0 Fail	77 x 3	Pass
PLTC	-55 to +150°C, Air, 1000hrs	0 Fail	77 x 3	Pass
uHAST	T=130°C, RH=85%	0 Fail	77 x 3	Pass
IOL	ΔTj ≥ 125℃; ton / toff = 1 min /5 min, 5000 Cycles	0 Fail	77 x 3	Pass
RSH	T=125°C bake 24hrs, T=30°C RH=60% soak 192hrs, 260±5℃, 10±1s	0 Fail	30 x 1	Pass
Solderability	Precondition Condition C (8hrs), Pb-free：245±5℃, 5±0.5s	0 Fail	10 x 1	Pass

3. Reliability Tests

Innoscience's E-mode GaN FETs were subjected to a variety of reliability test under the condition referenced to typical for silicon-based power MOSFETs. These test items and results were shown as below:

High Temperature Reverse Bias (HTRB)

Parts were subjected to 100% of the rated drain-source voltage at the maximum rated temperature for a stress period of 1000 hours. The testing was done in accordance with the JEDEC Standard JESD22-A108.

Pass criteria: All units must pass the min/max limits of the datasheet.

Test Item	Product Number	Test Condition	#Fail	Sample Size (Unit x Lot)	Duration (Hrs)
HTRB	INN100EA035A	T=150°C, VD=100V, VG=VS=0V	0	77 x 3	1000

Low Temperature Reverse Bias (LTRB)

Parts were subjected to 100% of the rated drain-source voltage with the ambient temperature of -40°C for a stress period of 1000 hours. The testing was done in accordance with the Qual. Plan

Test Item	Product Number	Test Condition	Fail #	Sample Size (Unit x Lot)	Duration (Hrs)
LTRB	INN100EA035A	Ta=-40°C, VD=100V, VG=VS=0V	0	77 x 3	1000

High Temperature Gate Bias (HTGB)

Parts were subjected to 100% of the rated positive gate-source voltage at the maximum rated temperature for a stress period of 1000 hours. The testing was done in accordance with the JEDEC Standard JESD22-A108.

Pass criteria: All units must pass the min/max limits of the datasheet.

Test Item	Product Number	Test Condition	#Fail	Sample Size (Unit x Lot)	Duration (Hrs)
HTGB	INN100EA035A	T=150°C, VG=6V, VD=VS=0V	0	77 x 3	1000

High Temperature Gate Bias (HTGB-)

Parts were subjected to 100% of the negative gate-source voltage at the maximum rated temperature for a stress period of 1000 hours. The testing was done in accordance with the Qual. plan.

Test Item	Product Number	Test Condition	#Fail	Sample Size (Unit x Lot)	Duration (Hrs)
HTGB-	INN100EA035A	T=150°C, VG=-4V, VD=VS=0V	0	77 x 3	1000

Low Temperature Gate Bias (LTGB)

Parts were subjected to 100% of the positive gate-source bias with the ambient temperature of -40°C for a stress period of 1000 hours. The testing was done in accordance with the Qual. plan.

Test Item	Product Number	Test Condition	#Fail	Sample Size (Unit x Lot)	Duration (Hrs)
LTGB	INN100EA035A	T=-40°C, VG=6V, VD=VS=0V	0	77 x 3	1000

Low Temperature Gate Bias (LTGB-)

Parts were subjected to 100% of the negative gate-source bias with the ambient temperature of -40°C for a stress period of 1000 hours. The testing was done in accordance with the Qual. plan.

Test Item	Product Number	Test Condition	#Fail	Sample Size (Unit x Lot)	Duration (Hrs)
LTGB-	INN100EA035A	T=-40°C, VG=-4V, VD=VS=0V	0	77 x 3	1000

Electro-Static Discharge (ESD)

Parts were subjected to HBM (ESDA/JEDEC JS-001) and CDM (ESDA/JEDEC JS-002) test to guarantee that the device can with stand electrostatic voltages during handling.

Pass criteria: All units must pass the min/max limits of the datasheet.

Test Item	Product Number	Test Condition	Sample Size (Unit x Lot)	JEDEC Class
HBM	INN100EA035A	T=25°C, All Pins	10 x 1	Class 1B
CDM	INN100EA035A	T=25°C, All Pins	10 x 1	Class C2a

Dynamic High Temperature Operating Life (DHTOL)

Parts were subjected to hard switch and soft switch system test adapted DHTOL H-bridge topology with V_{IN} =80V bias and F_{SW}=100kHz and 500kHz at junction temperature at 125°C for a stress period of 1000 hours. The testing was done in accordance with the standard JEP180.

Pass criteria: All units must pass the min/max limits of the datasheet.

Test Item	Product Number	Test Condition	#Fail	Sample Size (Set x Lot)	Duration (Hrs)
DHTOL	INN100EA035A	Hard switching, T=125°C, 100KHz, VD=80V	0	8 x 1	1000
	INN100EA035A	Hard switching, T=125°C, 600KHz, VD=80V	0	8 x 2	1000
	INN100EA035A	Soft Switching, T=125°C, 500KHz, VD=80V	0	8 x 1	1000
	INN100EA035A	Soft Switching, T=125°C, 1.5MHz, VD=80V	0	8 x 2	1000

Moisture Sensitivity Level (MSL)

Parts were baked at 125°C for 24 hours, and then subjected to 60%RH at 30°C for a stress period of 192 hours. The parts were also subjected to three cycles of Pb-free reflow in accordance with the IPC/JEDEC standard J-STD-020.

Pass criteria: All units must pass the min/max limits of the datasheet.

Test Item	Product Number	Test Condition	#Fail	Sample Size (Unit x Lot)	Duration (Hrs)
MSL3	INN100EA035A	T=30°C, RH=60%, 3 x reflow	0	25 x 3	192

High Humidity, High Temperature Reverse Bias (H3TRB)

Parts were subjected to 80% of the rated drain-source bias at 85%RH and 85°C for a stress period of 1000 hours. The testing was done in accordance with the JEDEC Standard JESD22-A101.

Pass criteria: All units must pass the min/max limits of the datasheet.

Test Item	Product Number	Test Condition	#Fail	Sample Size (Unit x Lot)	Duration (Hrs)
H3TRB	INN100EA035A	T=85°C, RH=85%, VD=80V, VG=VS=0V	0	77 x 3	1000

Part Level Temperature Cycling (PLTC)

Parts were subjected to temperature cycling for a total of 1000 hrs. Heating rate and cooling rate of 15°C/min. Dwell time of 5 minutes were used in accordance with the JEDEC Standard JESD22-A104.

Pass criteria: All units must pass the min/max limits of the datasheet.

Test Item	Product Number	Test Condition	#Fail	Sample Size (Unit x Lot)	Duration (hrs)
PLTC	INN100EA035A	-55 to +150°C, Air	0	77 x 3	1000

Unbiased Highly Accelerated Temperature and Humidity Stress Test (uHAST)

Parts were subjected to 85%RH and 130°C for a stress period of 96 hours. The testing was done in accordance with the JESD22-A118 Standard.

Pass criteria: All units must pass the min/max limits of the datasheet.

Test Item	Product Number	Test Condition	#Fail	Sample Size (Unit x Lot)	Duration (Hrs)
uHAST	INN100EA035A	T=130°C, RH=85%	0	77 x 3	96

Intermittent Operating Life (IOL)

Parts are subjected to power cycled over ΔT=125°C temperature range. Devices are heated through internal electrical power dissipation with combined gate and drain bias, and a regulated drain current. With one minutes temperature ramp, and five minutes cool down for a stress period of 5000 cycles. The testing was done in accordance with the MIL-STD-750 (Method 1037).

Test Items	Part Number	Test Conditions	#Fail	Sample Size (SS x Lot)	Duration
IOL	INN100EA035A	ΔTj =125°C,Tjmax=150°C Ton/Toff=1min/5min	0	77 x 3	5000Cys

Resistance to Solder Heat (RSH)

Parts were subjected to solder immersion condition after bake, soak. The testing was done in accordance with the JESD22-A111 Standard.

Pass criteria: After test, there is no abnormal finding during visual inspection, and all units must pass the min/max limits of the datasheet.

Test Item	Product Number	Test Condition	Sample Size (Unit x Lot)	#Fail
RSH	INN100EA035A	T=125°C bake 24hrs, T=30°C RH=60% soak 192hrs, 260±5℃, 10±1s	30 x 1	0 Fail

Solderability

Parts were subjected to surface mount process then reflow test. The testing was done in accordance with theJ-STD-002.

Pass criteria: Wetting area > 95%.

Test Item	Product Number	Test Condition	Sample Size (Unit x Lot)	#Fail
Solderability	INN100EA035A	1. Precondition: 8H 2. Pb-feee, 245±5°C, 5±0.5S.	10 x 1	0

Parts were mounted on to FR4 adaptor cards. Adaptor cards with two copper layers were used. The copper layer thickness was between 1 and 2 oz. SAC305 solder was used to mount the DUTs onto the adaptor cards.

Revision/Updated History

Revision	Reason for Change	Date	Prepared by	Approved by
1.0	Final release	Feb./11/2024	Huahui Wang Wanting Chen	Manager: Leilei Chen VP: Jianping Wang